# InCore Innovator Access Program

# What is I²AP?

InCore Innovator Access Program (I²AP) offers zero cost access to InCore's embedded series of RISC-V processors - the Azurite Series. This program allows startups to iterate and design with the Azurite core family without any upfront licensing fees. I²AP is designed to accelerate innovation by providing a scalable platform that eliminates barriers to embedded SoC design. With a tiered support system and production-based pricing, I²AP aims to foster a new wave of technological advancement in RISC-V solutions.

## Core Offering

**Azurite RISC-V core**

- 2-stage in-order 64/32-bit processor
- Optimized for low-power and resource-constrained applications
- Mid-range compute systems: 150-300 MHz
- Supports RV[64|32]IMACUBP ISA with PMP support
- JTAG-based debugging with non-invasive architecture
- Compares to M0 -> M4
- Silicon proven and integrated in customer projects

## Key benefits

- Zero upfront licensing fees
- Yearly subscription model
- Production-based pricing
- Tiered support system
- Comprehensive development tools and resources

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# What you get: Tiers, Tools and Pricing

## 1. Access and Licensing

- Startups receive full access to Azurite cores without upfront costs
- Annual subscription model for continued access and updates
- Licensing fees only apply when products enter production

## 2. Support tiers & deliverables

| Tier | Kickstarter | Advanced | Premium |
|---|---|---|---|
| **IP Portfolio** | Azurite series of processors (limited config set) | Everything in **Kickstarter**<br><br>+ Full Azurite configuration set<br><br>+ In-house SoC-subsystems based on Azurite*<br><br>+ Security/Crypto IPs | Everything in **Advanced**<br><br>+ Integration of third-party IPs<br><br>+ Custom accelerator integration<br><br>+ Custom instruction integration |
| **Support from InCore** | • Online documentation<br>• Email support (48-hr response time) | • Priority email support (24-hr response time)<br>• Monthly consultation calls | • Bespoke support - Dedicated support engineer<br>• Consultation for advanced micro-architectural configurations |
| **Number of tape-outs per year** | 1 | Unlimited | |
| **Configurations** | Limited CPU configurations (refer 'Azurite config tiers' section below) | Access to all ISA and Micro-Architectural configurations | |

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| Tools and models | SDK included<br>FPGA Reference SoC included | | |
|---|---|---|---|
| Subscription fee | $0 | $16,000 per annum | Contact Sales |

## 3. Tools and development Resources

- Access to Configurable IP.
- Access to RTL source.
- Comprehensive SDK and toolchain for reference platform.
- FPGA kit for reference platform.
- Documentation and application notes.
- Synthesis, Lint and Constraints collaterals.

## 4. From Prototype to Production: Pricing

- Transparent, volume-based pricing model (details shared upfront).
- Early adopter discounts for first-to-market products.

# What Sets I²AP Apart

1. **Zero means Zero**: Unlike other models, which may include some initial fees, I²AP offers completely free access for startups.

2. **Flexible Support Tiers**: Customizable support levels allow startups to scale their engagement as they grow, providing more value than the traditional one-size-fits-all approach.

3. **Open Architecture**: RISC-V based Azurite cores offer greater customization potential compared to competing offerings.

4. **Transparent Pricing**: Clear, predictable production pricing structure without hidden fees or complex terms.

5. **Ecosystem Empowerment**: Strong focus on building a collaborative ecosystem, fostering innovation beyond just core licensing.

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6. **Future-Proof Technology**: RISC-V architecture ensures long-term viability and freedom from geopolitical concerns that may affect alternate architectures.

# Azurite Configurations: Kickstarter to Premium

| | **Kickstarter** | **Advanced** |
|---|---|---|
| **Base ISA** | **RV32I/E + Zicsr** | |
| **Extensions** | <ul><li>M Extension (Integer Multiply/Divide)</li><li>C Extension (Compressed)</li><li>Zmmul (Only Integer Multiply)</li><li>Bit Manipulation Zba, Zbb, Zbc, & Zbs</li><li>Zicntr (Basic Counter Support)</li><li>Zifencei</li><li>Single Precision Floating Point F-Extension</li><li>Resumable Non-Maskable Interrupts (Smrnmi)</li><li>Zicsr (CSR Access)</li><li>Machine and User privilege Modes</li><li>PMP Support</li></ul> | <ul><li>*Advanced Configuration Assistance to meet different PPA requirements of the Extensions specified in the Kickstarter. Viz., iterative/fixed multipliers, retiming options etc.,*</li><li>RV64 support</li><li>Additional Bitmanipulation Extensions: (Zbp, Zbe, Zbr, Zbf, Zbt)*</li><li>Double Precision Floating Point D-extension</li><li>PSIMD/DSP Extensions (Zpn, Zpsf, Zbpbo)</li><li>Custom Performance Counters (Zihpm)</li></ul> |
| **Uncore Options** | <ul><li>Core Local Interrupt (CLINT) controller</li><li>PLIC (Upto 32 sources with limited priority levels)</li><li>Debug Module</li></ul> | <ul><li>Support for Custom Interrupts</li><li>Triggers Support (Sdtrig)</li></ul> |

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| **Misc. Options** | • Multiple Clock Domain/Reset Domain Support<br>• AXI4 Bus Support | • Multiple Hart Support<br>• AHB Bus support with customized bus configurations (Latency, Bandwidth)<br>• Entire Interconnect portfolio including protocol bridges, CDCs, Data crossings, etc. |
| **Memory Options** | • Split TCMs<br>  (OR)<br>• Separate L0 I$ and L0 D$ backed by an L2$ | • Higher Load-to-use Latency in TCMs for higher frequency closure |
| **Additional features/IP** | • UART, I2C, SPI, JTAG<br>• GPIO, PWM, WatchDog<br>• OnChip RAM, ROM<br>• DMA, WatchDog | **Security IPs**<br>• AES, SHA, ECC, RSA<br>• BigNum Accelerator<br>• Secure Keystore<br>• SecureBoot |

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# Premium Pack:

Everything in Advanced **+ a whole lot of customization to build your bespoke Azurite based subsystem.**

*For more details on the program, our cores & other offerings,* **contact sales: info@incoresemi.com**
1. *Cores - https://incoresemi.com/products/core-generator/*
2. *Reference SoC designs - https://incoresemi.com/products/custom-socs/*

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